**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1-12. (Cancelled)

13. (New) A scan line circuit that solves screen flicker, imperfect exposure junctions and inhomogeneous brightness in a TFT-LCD, which includes a plurality of perpendicular scan lines and a plurality of horizontal data lines, each of the scan lines connecting a plurality of pixel TFTs in a row and each of the data lines connecting a plurality of pixel TFTs in a column to form an array of the pixel TFTs, and a drain of the each pixel TFTs connecting a liquid crystal capacitor and a storage capacitor, wherein each of the scan line comprises:

gate voltage deformation means for deforming a gate input voltage waveform input from an input terminal of the scan line, the gate voltage deformation means located only between the gate of the first pixel TFT in the row and the input terminal of the scan line.

14. (New) The circuit of claim 13, wherein the gate voltage deformation means comprises a resistor.

15. (New) The circuit of claim 14, wherein the resistance of the resistor is in the range between 10 Ω/sq and 100 Ω/sq.

16. (New) The circuit of claim 13, wherein the gate voltage deformation means comprises an ITO thin film.

17. (New) The circuit of claim 13, wherein the gate voltage deformation means comprises a TFT that the TFT's gate connects the TFT's source directly.

18. (New) A scan line circuit that solves screen flicker, imperfect exposure junctions and inhomogeneous brightness in a TFT-LCD, which includes a plurality of perpendicular scan lines and a plurality of horizontal data lines, each of the scan lines connecting a plurality of pixel TFTs in a row and each of the data lines connecting a plurality of pixel TFTs in a column to form an array of the pixel TFTs, and a drain of the each pixel TFTs connecting a liquid crystal capacitor and a storage capacitor, wherein each of the scan line comprises:

gate voltage deformation means for generating a deformed gate voltage waveform transmitted to the pixel TFTs connected to the same scan line, the gate voltage deformation means located between the gate of the first pixel TFT in the row and the input terminal of the scan line.

19. (New) The circuit of claim 18, wherein the gate voltage deformation means comprises a resistor.

20. (New) The circuit of claim 19, wherein the resistance of the resistor is in the range between 10 Ω/sq and 100 Ω/sq.

21. (New) The circuit of claim 18, wherein the gate voltage deformation means comprises an ITO thin film.

22. (New) The circuit of claim 18, wherein the gate voltage deformation means comprises a TFT that the TFT's gate connects the TFT's source directly.